Notice of Allowability	Application No.	Applicant(s)	
	09/867,375	BERTSCH ET AL.	
	Examiner	Art Unit	
	Ayal I Sharon	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Amendment filed 1/19/2005*.

2. ☒ The allowed claim(s) is/are *1-36*.

3. ☒ The drawings filed on *8/17/2001* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER

DETAILED ACTION

Introduction

1. Claims 1-36 of U.S. Application 09/867,375, originally filed on 10/4/2004 are presented for examination. Applicants have amended claims 1-2, 4-9, 16, 18, 23, 30, and 33-36. Claims 24-29 were allowed in the previous Office Action. Claims 8, 18, and 23 were indicated as having allowable subject matter. The independent claims are 1, 8-9, 16, 18, 23 and 30.

Claim Interpretation

2. Examiner interprets the claimed "Geometric Parameters" correspond to the parameters listed in the table next to paragraph 22 of the specification: "Effective Transistor Channel Length", "Gate Oxide Thickness", "Change in Device Width."
3. Examiner interprets the claimed "DC Parameters" correspond to the parameters listed in the table next to paragraph 22 of the specification: "Saturated Source / Drain Current", "Saturation Threshold Voltage", and "Linear Threshold Voltage".
4. Examiner interprets the claimed "AC Parameters" correspond to the parameters listed in the table next to paragraph 22 of the specification: "Overlap Capacitance", "Source/Drain Junction Capacitance", and "Sheet Resistance."

5. Examiner interprets the claimed "Delay Parameters" as corresponding to the parameter listed in the table next to paragraph 22 of the specification: "Delay per stage of Kerf Performance Screen Ring Oscillator."

Examiner's Statement of Reasons for Allowance

6. The following is an examiner's statement of reasons for allowance.
7. In the previous Office Action, the cited prior art was:
   a) Strojwas, A.J., "Design for Manufacturability and Yield". Proc. of the 26th ACM/IEEE Conf. on Design Automation. 1989. pp.454-459. (Henceforth referred to as "**Strojwas**").
   b) Michael, C. et al. "A Flexible Statistical Model for CAD of Submicrometer Analog CMOS Integrated Circuits." Proc. of the 1993 IEEE/ACM Int'l Conf. on CAD. 1993. pp.330-333. (Henceforth referred to as "**Michael**").
   c) Bryant et al., U.S. Patent 6,239,591. (Henceforth referred to as "**Bryant**").
8. In the previous Office Action, Claims 24-29 were allowed.
   a) Claim 24 was allowed because neither the Strojwas reference, the Michael reference, nor the Bryant reference expressly teach the specific sequence of comparing and correcting steps recited in the claim.
   b) Claims 25-28 depend from Claim 24, and therefore were also allowed for the same reasons as for Claim 24.
   c) Claim 29 was allowed because neither the Strojwas reference, the Michael reference, nor the Bryant reference teach:

I. Removing defective chips from the first parameters to make a first set of go-data;

II. The specific sequence of comparing and correcting steps recited in the claim.

9. In the previous Office Action, Claims 8, 18-22, and 23 were objected to as being dependent upon a rejected base claim.

a) In regards to Claims 8 and 23, Examiner found that neither Strojwas, Michaels, or Bryant, individually or in combination, expressly taught the removing of defective devices from the test parametric data, as recited in the following limitations:

> 8. The method in claim 1, further comprising identifying defective devices and removing said defective devices from said in-line test parametric data.
>
> 23. The method in claim 16, further comprising, after said extracting, removing defective chips from said first parameters to make said first set of go-data.

b) In regards to Claim 18, Examiner found that neither Strojwas, Michaels, or Bryant, individually or in combination, expressly teach the following limitation:

> 18. The method in claim 17, further comprising calculating a percentage error based on said second comparing process and adding said percentage error to said second set of go-data to make a third set of go-data.

c) Claims 19-22 all depend from Claim 18, and therefore were objected to for the same reasons as Claim 18.

10. In the amendment filed 1/19/2005, Applicants amended claims 8, 18, and 23 to stand alone as independent claims.

11. Moreover, in the same amendment, the Applicants amended independent claims 1, 9, 16, and 30 to respectively include the following limitations:

1. ... removing defective devices from said test parametric data ...

9. ... measuring features of non-defective ones of said devices to produce measured features ...

16. ... removing defective chips from said first set of go-data ...

30. ... removing defective devices from said test parametric data ...

12. In an updated search, Examiner has found two additional references that are relevant to the limitation of "removing defective devices from parametric data", and variations of this limitation, as recited in independent claims 1, 8, 9, 16, 23, 29, and 30. These two additional references are:

a) Van Zant, P. Microchip Fabrication: A Practical Guide to Semiconductor Processing. ISBN 0-07-135636-3. © 2000. Chapter 15. (Henceforth referred to as "**Van Zant**").

b) Rajsuman, R. System-on-a-Chip: Design and Test. ISBN 1-58053-107-5. © 2000. Chapters 4 and 9-11. (Henceforth referred to as "**Rajsuman**").

13. The Van Zant reference (See p.490) teaches the following (emphasis added):

> A first step in process control is to make a histogram of the particular process parameter and determine if the distribution is a normal distribution. If it is not, the chances, the chances are good that there is something wrong with the process. If the distribution is a normal one, the next step is to **compare the range of the distribution with the design limits** for the particular parameter (Fig. 15.13). This comparison is made to determine if the natural process distribution limits fall within the design limits. **If they do not, the process must be fixed or some percentage of the parameter readings (and the wafers) wil always be out of specification.**

> Another useful statistical tool is the Pareto chart. This is a form of the histogram, but with the *x* axis divided into unrelated sections rather than a continuum of some parameter such as sheet resistance. **Defect inspection results are a good candidate for Pareto charts.** On the *x* axis is a list of defect categories. A mark or vertical column over each defect type indicates the frequency of occurrence of each defect types. **The operator or process engineer can see from the chart which defects are occurring most often and what processes must be improved.**

The claimed invention therefore teaches away from the Van Zant reference, because the Van Zant reference preserves the defective devices in the parametric data in order to:

a) Compare the production distribution to the design limits (See p.490, and Fig.15.13)

b) "Improve" and "fix" the production processes (See p.490).

The claimed invention, on the other hand, removes defective device data from the test parametric data before comparing the test parametric data to the simulation models. Therefore, by removing defective devices from the test data (as in the claimed invention), neither of the benefits taught by Van Zant can be attained.

14. The Rajsuman reference teaches (see pp.101-102, section 4.3.3 Hardware Prototypes) the following (emphasis is from the original text):

> Despite the best attempts by engineers to make the first silicon fully functional, only about 80% of designs work correctly when tested at the wafer level, and more than half fail when put into the system for the first time. The primary reason is the lack of system-level testing with a sufficient amount of real application runs. The only means to do it with present-day technology is by using either FPGA/LPGA or ASIC silicon prototypes.

> ... However, deciding when to use silicon is an important decision because producing a silicon prototype is a costly proposition. These factors should be considered:
>
> 1. *The diminishing bug rate in verification and cosimulation.* When the basic bugs have been eliminated, an extensive application run will be required to find other bugs. Cosimulation and emulation may not be able to run an application for extensive time periods.
>
> 2. *The difficulty of finding bugs.* If finding a bug takes a few orders of magnitude more time than the time required to fix it, then a silicon prototype is very useful because it finds bugs quickly.
>
> 3. *The cost (manual effort, time-to-market) of finding bugs.* If the search for bugs with the cosimulation or emulation methods is extremely costly, then silicon prototyping should be considered.

Rajsuman therefore is teaching that the purpose of the test parametric data is to find defects (bugs), which are inherently found by comparing test results to the specification models. This therefore teaches away from the claimed invention, which removes defective devices from the test parametric data.

15. The Rajsuman reference also teaches (see pp.239-240, section 10.1 Production Test Flow) the following (emphasis added):

> During the production of ICs, each chip is tested multiple times with electrical AC, DC, and parametric tests. Whereas the packaged part is subjected to all tests, at the wafer level a subset of tests is used. Two examples of production test flow are given in Figure 10.1. A typical after wafer completion may contain the following steps:
>
> 1. *Wafer sort testing:* This type of testing contains parametric, functional, analog, and memory tests. Normally the specified junction temperature (T_j) for wafer sort is 75°. Large memories (such as megabit DRAM and flash memories) in SoC are tested extensively at this stage with multiple test patterns. **All memory failures are identified. This is followed by redundancy analysis and repair. After repair another memory test is performed to ensure that there are no more memory failures.**

Rajsuman therefore is teaching that the purpose of the test parametric data is to find defects (bugs), which are inherently found by comparing test results to the specification models. This therefore teaches away from the claimed invention, which removes defective devices from the test parametric data.

16. In the continuation of the above cited section of Rajsuman, the reference teaches (see p.239-240, section 10.1 Production Test Flow) the following:

> 3. *First package level test:* This testing contains parametric and functional tests including a simple test of memory and analog/mixed-signal circuits such as PLL and DACs. The main objective of this test is to filter failures that occurred during packaging.
>
> 5. *Second package level test:* This is considered the most important test. It contains all parametric, functional, stuck-at logic (scan, BIST, and so on), full memory and analog/mixed-signal, and Iddq testing. Many manufacturers also apply functional, stuck-at logic, full memory, and analog/mixed-signal tests at more than one voltage level, such as at typical Vdd and at 15% higher voltage (1.15Vdd).

Rajsuman is again teaching that the purpose of the test parametric data is to find defects (bugs), which are inherently found by comparing test results to the specification models. This therefore teaches away from the claimed invention, which removes defective devices from the test parametric data, and compares simulating models to the test parametric data 9which no longer has defective device data).

17. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ayal I. Sharon whose telephone number is (571) 272-3714. The examiner can normally be reached on Monday through Thursday, and the first Friday of a biweek, 8:30 am – 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached at (571) 272-3716.

Any response to this office action should be faxed to (703) 872-9306, or mailed to:

USPTO
P.O. Box 1450
Alexandria, VA 22313-1450

or hand carried to:

USPTO
Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Tech Center 2100 Receptionist, whose telephone number is (571) 272-2100.

Ayal I. Sharon

Art Unit 2123

March 17, 2005

KEVIN J. TESKA
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PATENT EXAMINER